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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,414	11/19/2003	Yuan-Jen Chao	4459-0159P	5322

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EXAMINER	
SHEETS, ELIJAH M	

ART UNIT	PAPER NUMBER
2609	

NOTIFICATION DATE	DELIVERY MODE
05/18/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/715,414	CHAO, YUAN-JEN	
	Examiner	Art Unit	
	Eli M. Sheets	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/19/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/19/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in **Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966)**, that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: ***(See MPEP Ch. 2141)***

a. Determining the scope and contents of the prior art;
b. Ascertaining the differences between the prior art and the claims in issue;
c. Resolving the level of ordinary skill in the pertinent art; and
d. Evaluating evidence of secondary considerations for indicating obviousness or nonobviousness.

2. Claims 1-7 and 10-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al. (US 6,420,839 B1) in view of Lin et al. (US 6,856,519 B2).

Regarding claim 1, Chiang discloses a driving system for multiple lamps (plurality of lights), in which multiple transformers (plurality of oscillation step-up circuits) may be used depending on the number of lamps to be driven (Col. 3, lines 39-41). However, Chiang fails to disclose a digital control circuit for the driving system. Lin teaches an inverter controller integrated circuit which operates to generate two-switch driving signals (digital signals) (Col. 2, lines 32-33), which transmits output to transformer circuits (oscillation step-up circuits) (Fig. 3, 4). In addition, the controller sets digital switching signal pulse width (phase and duty cycle) (Col. 2, line 60). Therefore, it would have been obvious to one of ordinary skill in the art at the

time of invention to combine the teachings of Chiang and Lin for the benefit of reducing the overall pin count and reducing the number of components without reducing the functionality and/or performance of the controller (Col. 1, lines 7-10).

Regarding claim 2, combination of Chiang and Lin further discloses that multiple transformers (Chiang, oscillation step-up circuits) may be used depending on the number of lamps to be driven (Chiang, each of the step-up circuits connected to at least one of the lights).

Regarding claim 3, combination of Chiang and Lin discloses CCFL lamps for loads in his inverter controller (Lin, Col. 2, line 57).

Regarding claim 4, combination of Chiang and Lin discloses (Lin, in Fig. 3 and 4) an oscillation step-up block in which two switches, namely Q1 and Q2, comprise a switching unit, and transformer 60 comprises a resonance step-up unit. As can be seen in the figures, the switching unit connects directly to the digital control circuit 10, and receives gate signals (performs switching), output from the control circuit. In addition, the transformer leads are connected to the transistors of the switching unit, and the transformer controlled by these transistors.

Regarding claim 5, combination of Chiang and Lin discloses (Lin, in Fig. 3 and 4) that the resonance step-up unit comprises a capacitor 68 and a transformer 60.

Regarding claim 6, combination of Chiang and Lin discloses (Lin, in Fig. 3 and 4) that the switching unit comprises two transistors (Q1 and Q2), which connect to the two ends of the capacitor, and that the transistor gates receive switching control signals (turn on/off) from the digital control unit 10.

Regarding claim 7, combination of Chiang and Lin teaches (Lin, in Fig. 3 and 4) that the transistors (Q1 and Q2) of the switching unit are MOS transistors.

Regarding claim 10, combination of Chiang and Lin teaches a controller which operates to generate two switch-driving signals (Lin, generates the sets of the digital switching signals) (Lin, Col. 2, lines 32-33) which electrically connects to oscillation step-up circuit (respectively input to the oscillation step-up circuits) (Lin, Fig. 3 and 4). In addition, it also teaches that the controller (Lin, multiplex feedback-control calculating circuit), includes a current feedback control circuit and a MUX (multiplexor) (Lin, Col 2., lines 24-26). The intersection between a sawtooth signal and an error signal is used by the switch driver logic to set the pulse width (Lin, duty cycles of the sets of the digital switching signals) of each of the driver (Lin, digital switching signal generating circuit) signals, and the value of the error signal is determined by current feedback information (according to feedback signals from the lights) (Lin, Col. 2, lines 58-67).

Regarding claim 11, combination of Chiang and Lin discloses that the inverter controller (multiplex feedback-control calculating circuit) takes the form of an integrated circuit (digital single-chip microprocessor) (Lin, Col. 1, lines 36-37).

Regarding claim 12, combination of Chiang and Lin teaches that the inverter controller includes a MUX (multiplex unit) (Col 2 line 26) that connects to the light (each of the lights) (Lin, Fig. 3 and 4). Also, the controller (electrically connected to the multiplex unit) receives feedback to determine if the load (from the lights) is operating properly (detecting unit) (Lin, Col 4, lines 22-24). In addition, Lin discloses that an amplifier compares the load current (analog feedback signal) to a user-definable reference signal indicative of maximum load current at

maximum power or maximum brightness. If the value of the load current is less than the reference signal, amplifier will source current to charge the capacitor in an attempt to increase the DC value of the error signal, thereby increasing the pulse width of the output driver signals (digital signals). If the value of the load current is greater than the reference signal, amplifier will sink charge from the CMP capacitor to decrease the DC value of the error signal, thereby decreasing the pulse width of the output driver signals (A/D conversion, control-calculating) (Lin, Col. 3, lines 6-20).

Regarding claim 13, Official notice is taken that the use of a plurality of signal detecting units as opposed to the single signal detecting unit of claim 12 is notoriously used in the art and would have been obvious to one skilled in the art at the time of invention for the benefit of feedback signal separation.

Regarding claim 14, combination of Chiang and Lin discloses that the controller (multiplex feedback-control calculating circuit) takes the form of an integrated circuit (digital single-chip microprocessor) (Lin, Col. 1, lines 36-37). In addition, Official notice is taken that the use of a plurality of signal detecting units as opposed to the single signal detecting unit of claim 12 is notoriously used in the art and would have been obvious to one skilled in the art at the time of invention for the benefit of feedback signal separation.

Regarding claim 15, combination of Chiang and Lin teaches that his controller is in the form of an integrated circuit (digital single-chip microprocessor). In addition, Lin teaches that the inverter controller includes a MUX (multiplex unit) (Lin, Col. 2, line 26) that connects to the light (each of the lights) (Lin, Fig. 3 and 4). Also, the controller (electrically connected to the multiplex unit) receives feedback to determine if the load (from the lights) is operating properly

(detecting unit) (Lin, Col 4, lines 22-24). In addition, Lin discloses that an amplifier compares the load current (analog feedback signal) to a user-definable reference signal indicative of maximum load current at maximum power or maximum brightness. If the value of the load current is less than the reference signal, amplifier will source current to charge the capacitor in an attempt to increase the DC value of the error signal, thereby increasing the pulse width of the output driver signals (digital signals). If the value of the load current is greater than the reference signal, amplifier will sink charge from the CMP capacitor to decrease the DC value of the error signal, thereby decreasing the pulse width of the output driver signals (A/D conversion, control-calculating) (Lin, Col. 3, lines 6-20).

Regarding claim 16, combination of Chiang and Lin teaches that the inverter controller includes a MUX (multiplex unit) (Lin, Col. 2, line 26) that is connected integrally to the detector unit (Fig. 3 and 4). In addition, Lin teaches that the controller is an IC, which is connected integrally to the multiplex unit (Fig. 3 and 4), and that the intersection between a sawtooth signal and an error signal is used by the switch driver logic to set the pulse width (duty cycles of the sets of the digital switching signals) of each of the driver (digital switching signal generating circuit) signals, and the value of the error signal is determined by current feedback information (according to feedback signals from the lights) (Lin, Col. 2, lines 58-67).

Regarding claim 17, combination of Chiang and Lin teaches that his controller is an integrated circuit (digital single-chip microprocessor), and that the IC includes an amplifier that compares the load current (analog feedback signal) to a user-definable reference signal indicative of maximum load current at maximum power or maximum brightness. If the value of the load current is less than the reference signal, amplifier will source current to charge the capacitor in

an attempt to increase the DC value of the error signal, thereby increasing the pulse width of the output driver signals (digital signals). If the value of the load current is greater than the reference signal, amplifier will sink charge from the CMP capacitor to decrease the DC value of the error signal, thereby decreasing the pulse width of the output driver signals (A/D conversion unit, control-calculating unit) (Lin, Col. 3, lines 6-20).

Regarding claims 18 and 19, combination of Chiang and Lin discloses that when the controller is initially powered on to drive a load, the controller will receive both load voltage (voltage signals) and load current (current signals) feedback to determine if the load is operating correctly (Lin, Col. 4, lines 22-24).

3. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al. (US 6,420,839 B1) in view of Lin et al. (US 6,856,519 B2), and further in view of Fujimura et al. (US 5,495,405).

Regarding claim 8, the combination of Chiang and Lin as a whole fails to teach an inverter circuit topology for driving a discharge tube, which uses bipolar junction transistors as switches in the switching network that serves as a control to the capacitor/transformer step-up circuit. However, Fujimura does (Fig. 1 and 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Chiang, Lin and Fujimura for the benefit of switching action, which is well known in the art.

Regarding claim 9, the combination of Chiang and Lin as a whole fails to teach the limitations as claim. However, Fujimura teaches that the topology of the switching unit comprises two resistors (R1 and R2), which connect to base electrodes of bipolar transistors

(TR1 and TR2) on one end, and to signal leads (control circuit signals) on the other end (Fujimura, Fig. 1 and 2).

Contact

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eli Sheets whose telephone number is (571) 270-1189. The examiner can normally be reached on M-F 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vu Le can be reached on (571) 272-7332. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-7332.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Elijah Sheets

VU LE
SUPERVISORY PATENT EXAMINER